4.3 Expansion Unit

The expansion unit is used for additional installation of RAMs and ROMs in the HX-20, and can be attached to the expansion unit interface (CN7) for the HX-20. The expansion unit can mount RAMs and ROMs up to 32k bytes maximum, and is normally equipped with 16k bytes of RAMs. In mounting additional ROMs, part or all of the RAMs (16k bytes) that are the standard equipment of the expansion unit can be ignored by resetting the DIP switches and jumpers.

Thus, RAMs and ROMs can be added as suitable to a specific application.

Features of Expansion Unit

- The interface outputs address bus (16 lines), data bus (8 lines) and R/W signals in parallel so that the main CPU of the HX-20 can make direct access to the memories.
- No special power supply is required for the expansion unit because all the power that is necessary to drive it is supplied from the HX-20.
- The RAM area in the expansion unit can be backed up by the built-in batteries in the HX-20 so that, even if power is turned off, the programs (data) sotred in the RAMs of the expansion unit can be protected similar to the RAMs in the HX-20.
- Part of the RAM addresses and part or all of the ROM addresses in the expnasion unit overlap with the ROM addresses in the HX-20, so the addresses in the HX-20 and in the expansion unit are separately used through bank switching.

4.3.1 Hardware Composition

(1) The expansion unit consists of ROM and RAM select circuits and a bank control (bank switching) circuit. Fig. 4-27 shwos a block diagram of the expansion unit.

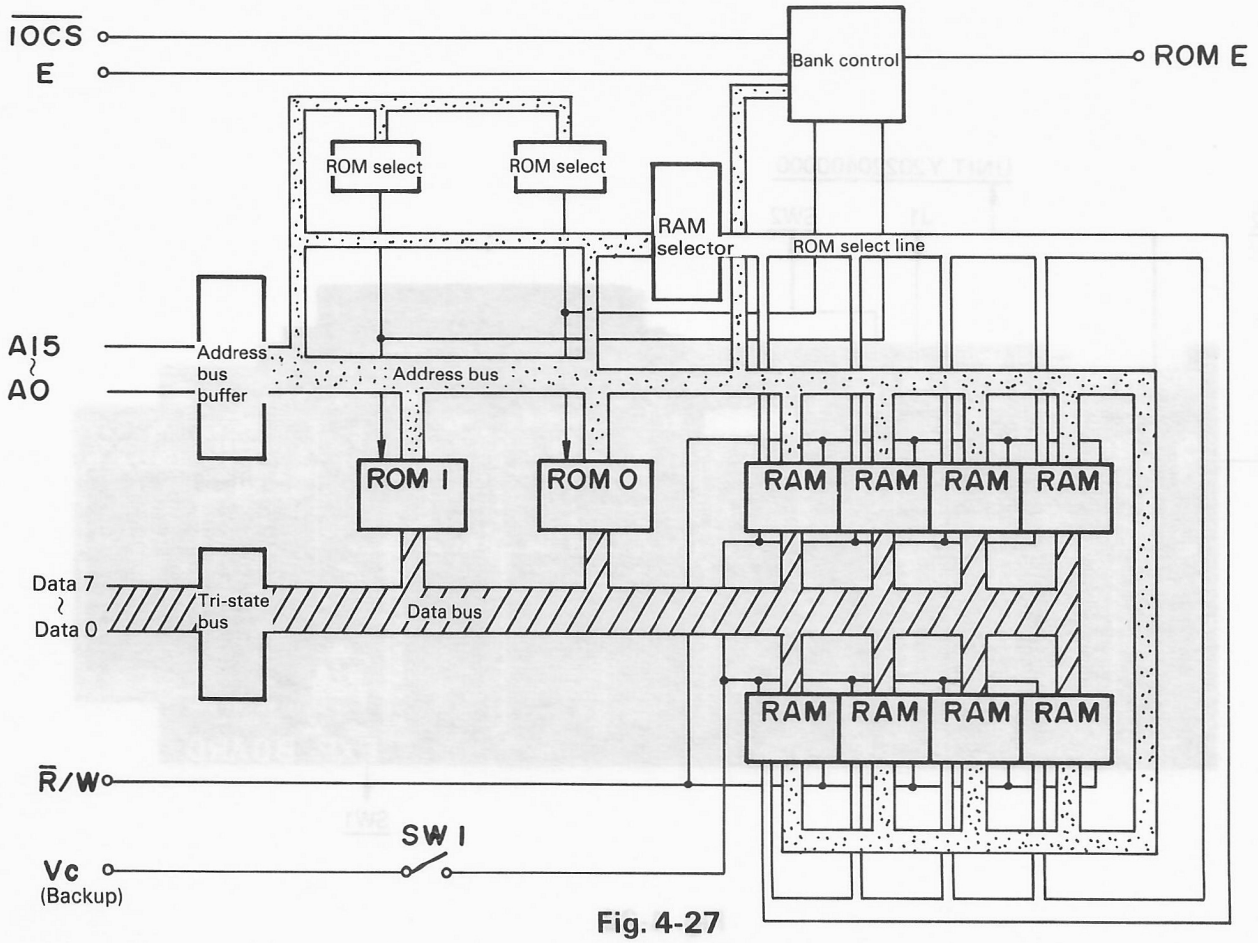
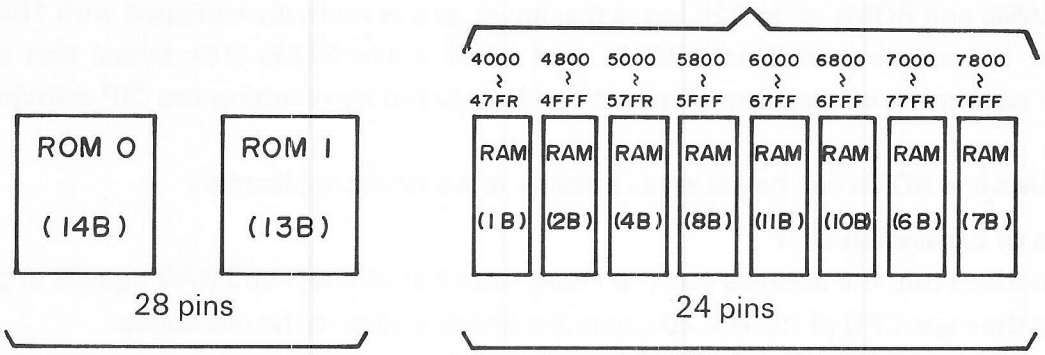


Fig. 4-27

(2) Expansion IC Socket

The expansion unit is normally equipped with 16k bytes of RAMs, and also has two 28-pin IC sockets for ROMs.



(2) RAM and ROM Composition

A total of 32k bytes maximum of RAMs and ROMs can be installed. ROM/RAM areas and types of ROMs (8KB/16KB) can be selected by means of the jumpers (J1, J2) and DIP switch (SW2) shown below.

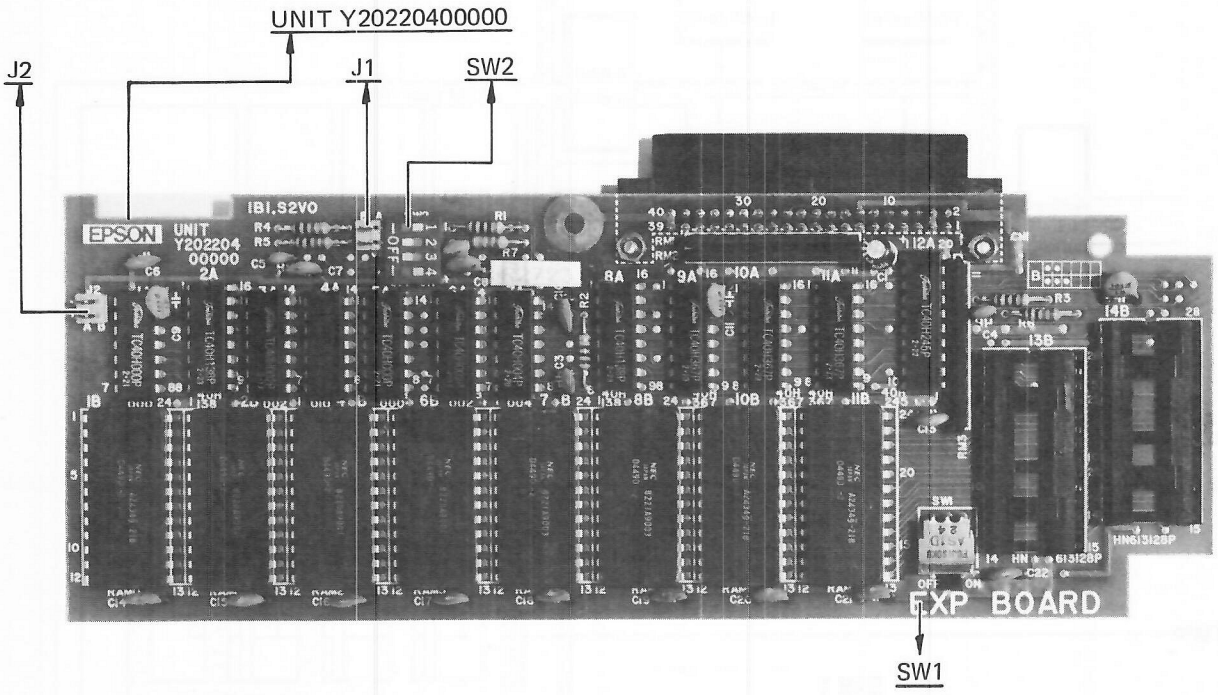


Fig. 4-28

4.3.2 ROM/RAM Select Circuits

● ROM select

Two expansion ROMs can be installed. ROM 0 (14B) is for the higher addresses, and ROM 1 (13B) for the lower addresses.

ROM addresses vary with ROM capacity (8k or 16k bytes) and quantity (1 ROM or 2 ROMs) so the circuit shown in Fig. 4-29 involving address A15 to A13, DIP switch (SW2) and jumper (J1/J2) is used for ROM selection.

For setting the DIP switch and reconnecting the jumper, refer to 4.3.3 Bank Switching and 4.3.5. Jumper (J1/J2) and DIP switch (SW1/2) Setting

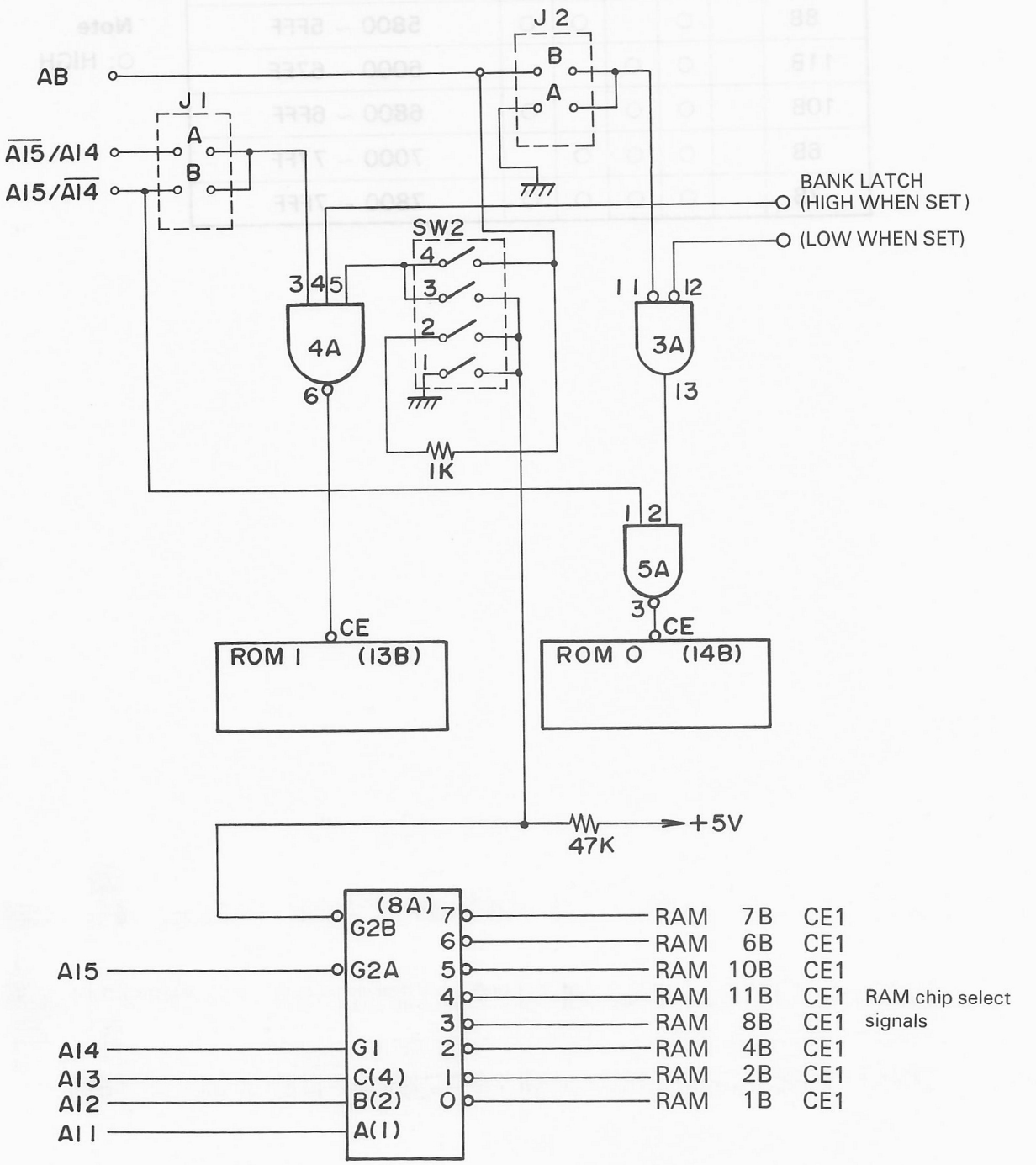


Fig. 4-29

● RAM selecting

RAM selection is basically performed by a decoder (IC 8A) using address lines A11 to A15. It is also controlled on the basis of DIP switch 2 setting because the range of addresses to be used must be changed depending on combination with ROMs.

Location	Address line					RAM address range
	15	14	13	12	11	
1B		○				4000 ~ 47FF
2B		○			○	4800 ~ 4FFF
4B		○		○		5000 ~ 57FF
8B		○		○	○	5800 ~ 5FFF
11B		○	○			6000 ~ 67FF
10B		○	○		○	6800 ~ 6FFF
6B		○	○	○		7000 ~ 77FF
7B		○	○	○	○	7800 ~ 7FFF

Note

○: HIGH

(Meanings of Jumpers and DIP Switch)

- SW2 bits 1 and 2 allocate ROM and RAM areas.
- SW2 bits 3 and 4 and jumpers J1 and J2 select a ROM capacity (8KB/16KB).

* Part or all of the 16k bytes of RAMs installed can be ignored by setting SW2 and the jumpers mentioned above.

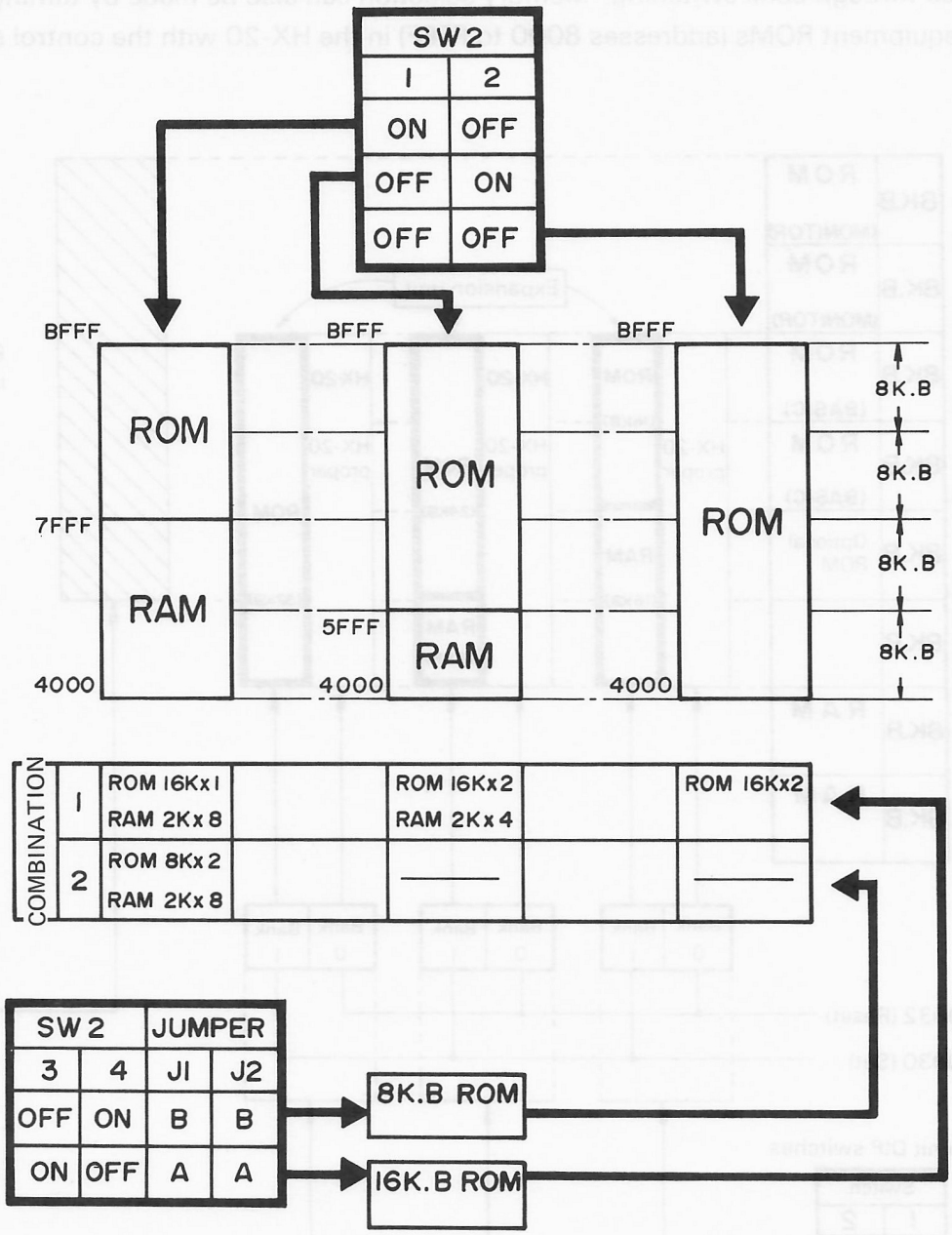


Fig. 4-30

4.3.3 Bank Switching

The HX-20 can directly select addresses up to 64k bytes (65,536 addresses). If the expansion unit is used, the total memory capacity of ROMs and RAMs may exceed 64k bytes.

However, the HX-20 can make access to memories having the same logic address through bank switching.

Memory selection by bank switching is done by hardware and sorfware. Since the HX-20 operates in the multiplexed/RAM mode, it can use external memories for addresses 00FF to FFFF. Thus, the addresses 4000 to BFFF (32k bytes in total) in the external memory area can be used through bank switching. Memory selection can also be made by turning off the standard equipment ROMs (addresses 8000 to FFFF) in the HX-20 with the control signal ROM E.

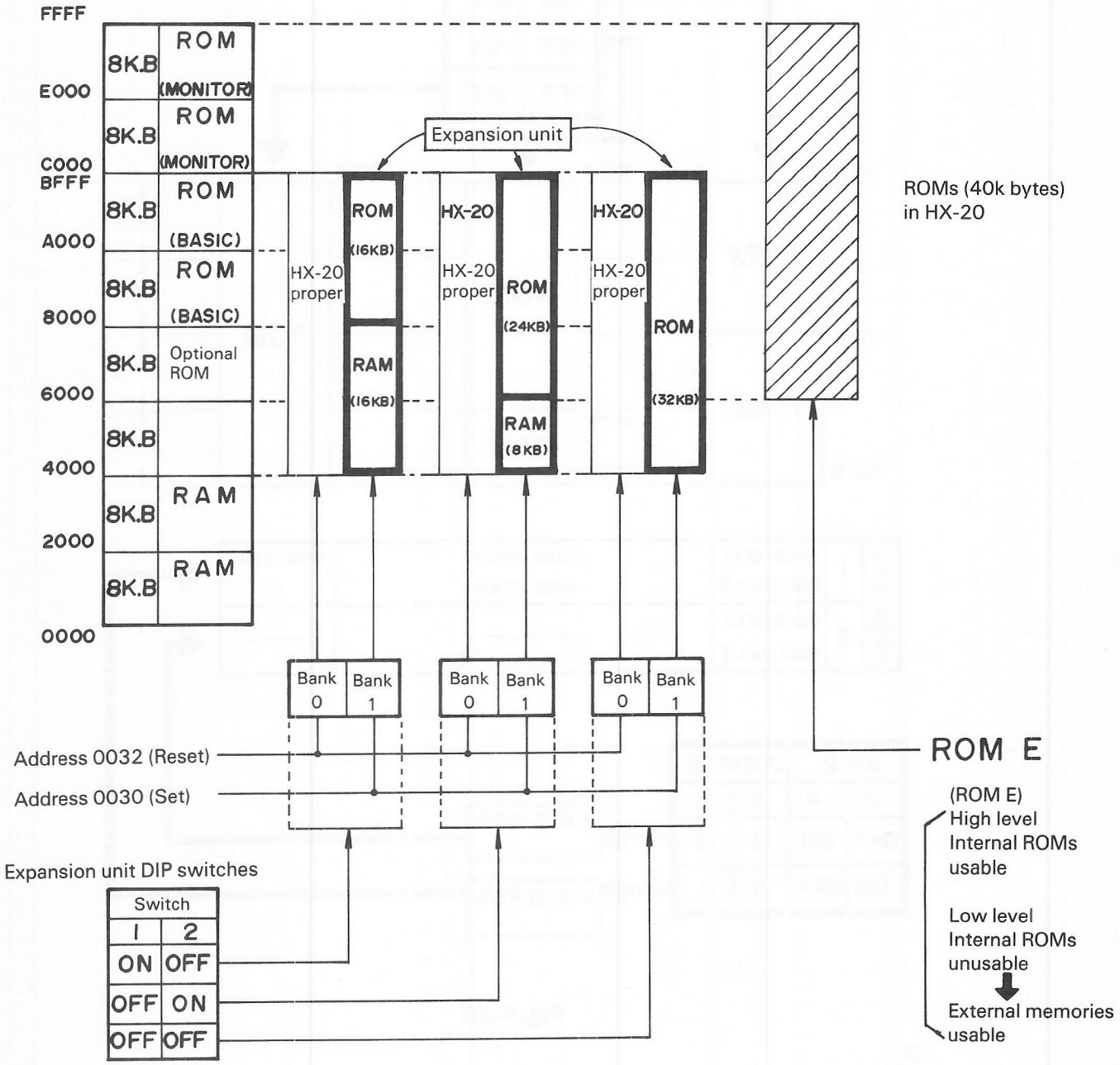


Fig. 4-31

● Bank switching is performed by a bank latch that uses address 0030 and 0032 and the ROM E signal based on control of address 14 and 15.

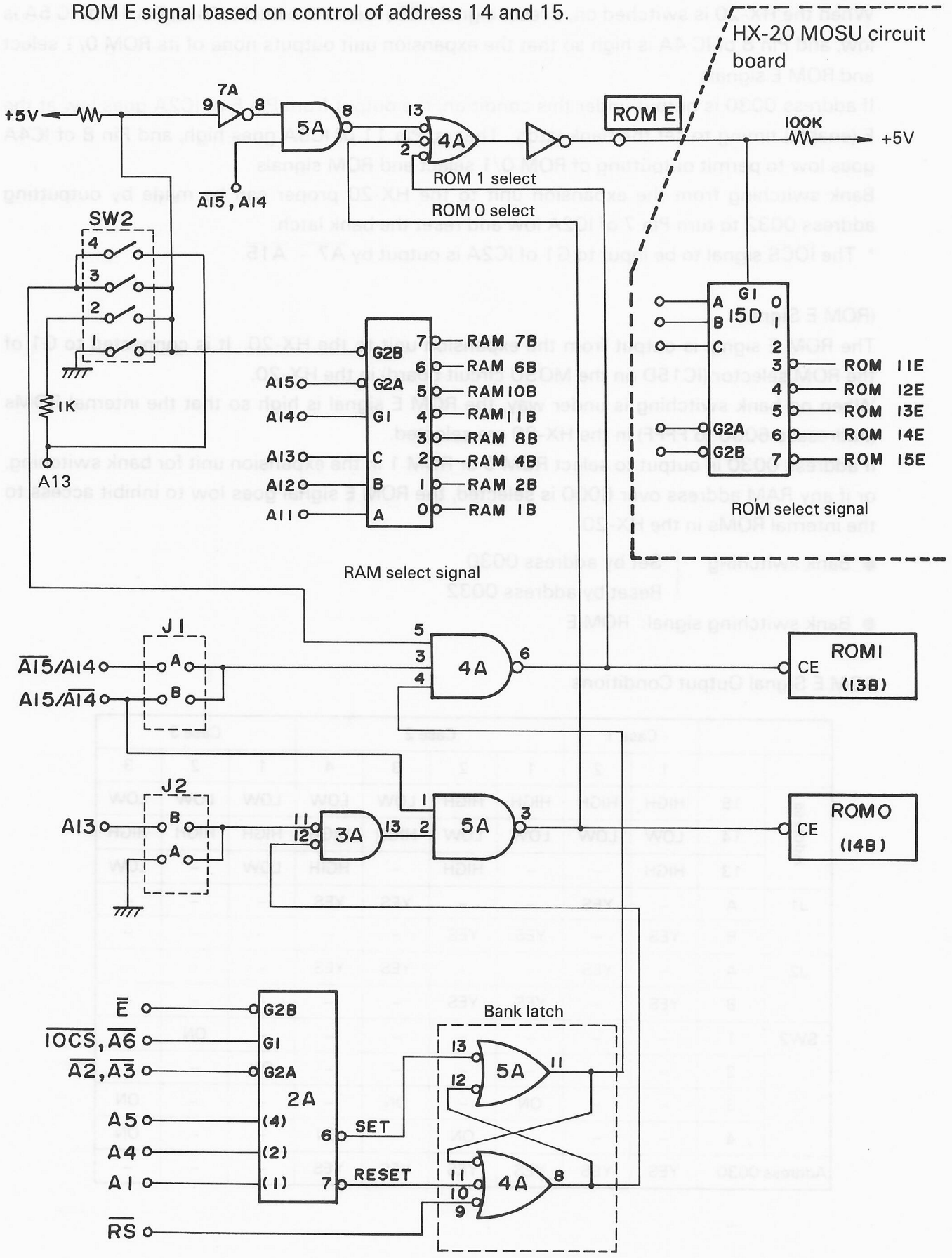


Fig. 4-32

(Bank Latch)

When the HX-20 is switched on, a reset signal ($\overline{RS}$) resets the latch. Thus, Pin 11 of IC 5A is low, and Pin 8 of IC 4A is high so that the expansion unit outputs none of its ROM 0/1 select and ROM E signals.

If address 0030 is output under this condition, the output from Pin 6 of IC2A goes low at the E (enable) timing to set the bank latch. That is, Pin 11 of IC5A goes high, and Pin 8 of IC4A goes low to permit outputting of ROM 0/1 select and ROM signals.

Bank switching from the expansion unit to the HX-20 proper can be made by outputting address 0032 to turn Pin 7 of IC2A low and reset the bank latch.

* The $\overline{IOCS}$ signal to be input to G1 of IC2A is output by $\overline{A7 \sim A15}$.

(ROM E Signal)

The ROM E signal is output from the expansion unit to the HX-20. It is connected to G1 of the ROM selector (IC15D on the MOSU circuit board) in the HX-20.

When no bank switching is under way, the ROM E signal is high so that the internal ROMs (addresses 6000 to FFFF) in the HX-20 are selected.

If address 0030 is output to select ROM 0 or ROM 1 in the expansion unit for bank switching, or if any RAM address over 6000 is selected, the ROM E signal goes low to inhibit access to the internal ROMs in the HX-20.

- Bank switching { Set by address 0030 / Reset by address 0032
- Bank switching signal: ROM E

ROM E Signal Output Conditions

		Case 1		Case 2				Case 3		
		1	2	1	2	3	4	1	2	3
Address	15	HIGH	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	LOW
	14	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
	13	HIGH	–	–	HIGH	–	HGIH	LOW	–	LOW
J1	A	–	YES	–	–	YES	YES	–	–	–
	B	YES	–	YES	YES	–	–	–	–	–
J2	A	–	YES	–	–	YES	YES	–	–	–
	B	YES	–	YES	YES	–	–	–	–	–
SW2	1	–	–	–	–	–	–	–	ON	–
	2	–	–	–	–	–	–	ON	–	–
	3	–	–	ON	–	ON	–	–	–	ON
	4	–	–	–	ON	–	ON	–	–	ON
Address 0030		YES	YES	YES	YES	YES	YES	–	–	–

The ROM E signal can be output under nine conditions.

Case 1: When ROM 0 (14B) in the expansion unit is selected

(1) Addresses 15, $\overline{14}$

(2) Bank 1 select (address 0030)

(3) Address 13 (when J2 = B)/or J2 = A

Case 2: When ROM 1 (13B) in the expansion unit is selected

(1) Address 15, $\overline{14}$ (when J1 = B)/or addresses $\overline{15}$, 14 (when J1 = A)

(2) Bank 1 select (address 0030)

(3) Address 13 (SW2-4 on)/or SW2-3 on

Case 3: When an address over 6000 in the expnasion unit's RAM is selected

(1) Addresses $\overline{15}$, 14

(2) Address $\overline{13}$ (SW2-2 on)/or address $\overline{13}$ (SW2-3, SW2-4 on), or SW2-1 on

4.3.4 Interface

- The data buses have IC12A (tri-state output), which switches data bus direction with read and write signals.

  If the $\overline{\text{ROM E}}$ signal is high at the E (enable) signal timing, data bus direction is switched by R/W signal timing.

(IC12A H245)

Read	A	←	B
Write	A	→	B

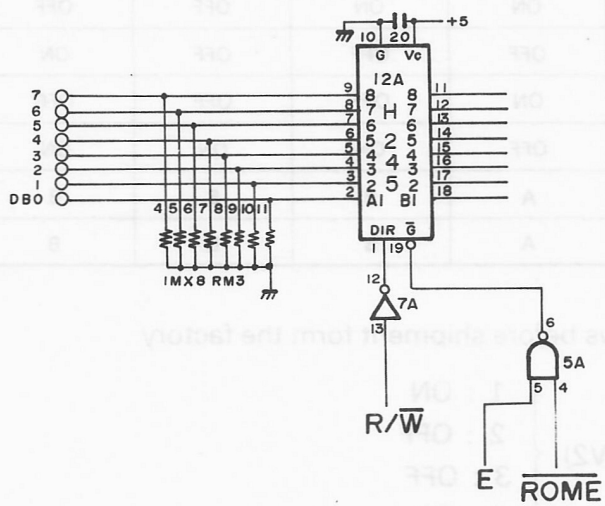
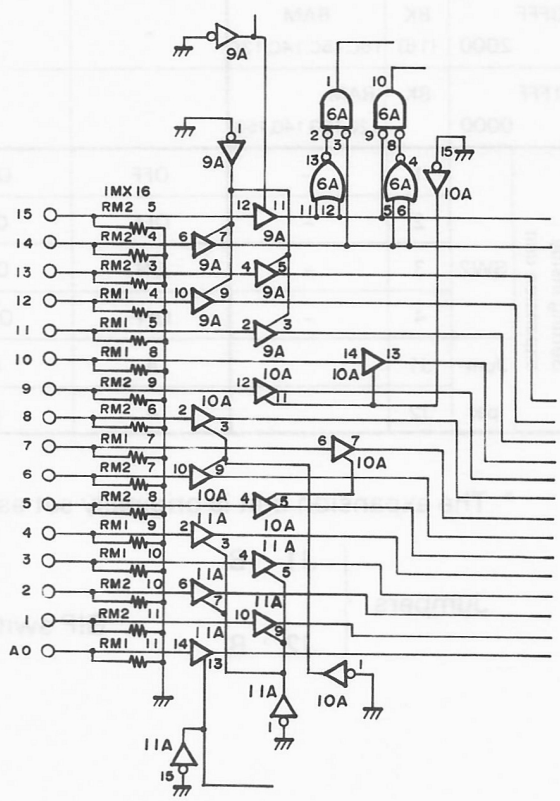


Fig. 4-33



4-34

- Address buses

  Address buses output addresses to each element via bus drivers IC9A, IC10A, and IC11A, which are connected so that each gate may be normally on. Thus, these ICs are immediately ready for operation when a +5V is supplied as power is turned on.

4.3.5 Jumper (J1/J2) and DIP Switch (SW1/2) Setting

- Part or all of the standard equipment of 16k bytes of RAMs can be ignored or replaced with ROMs by reconnecting the jumpers or setting DIP switches. Therefore, the expansion memory area can be used as shown in the table below without changing the standard equipment of 16k bytes of RAMs in the expansion unit.

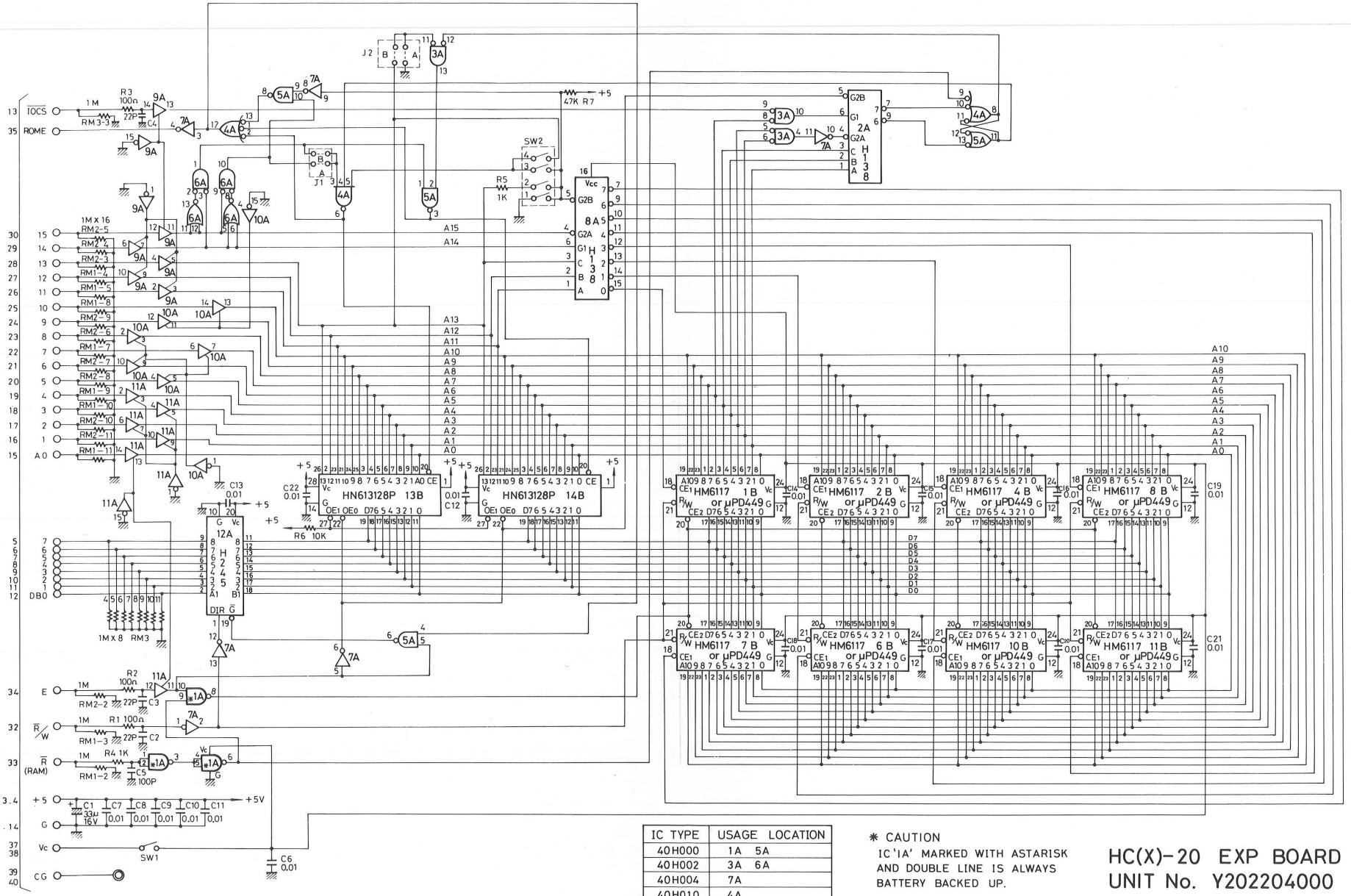
Address		Standard	ROM/RAM combination in expansion unit					
			16KB ROM × 2	16KB ROM × 2 2KB RAM × 4	16KB ROM × 1 2KB RAM × 8	8KB ROM × 2 2KB RAM × 8	8KB ROM × 2	8KB ROM × 2 2KB RAM × 4
FFFF E000	8K (64)	ROM (MONITOR) 15E	–	–	–	–	–	–
DFFF C000	8K (56)	ROM (UTILITY) 14E	–	–	–	–	–	–
BFFF A000	8K (48)	ROM (BASIC) 13E	ROM 0 (14B)	ROM0 (14B)	ROM 0 (14B)	ROM 0 (14B)	ROM 0 (14B)	ROM0 (14B)
9FFF 8000	8K (40)	ROM (BASIC) 12E				ROM 1 (13B)	ROM 1 (13B)	ROM 1 (13)
7FFF 6000	8K (32)	(Optional ROM)	ROM 1 (13B)	ROM 1 (13B)	RAM (11B,10B,6B,7B)	RAM (11B,10B,6B,7B)		
5FFF 4000	8K (24)			RAM (1B,2B,4B,8B)	RAM (1B,2B,4B,8B)	RAM (1B,2B,4B,8B)		RAM (1B,2B,4B,8B)
3FFF 2000	8K (16)	RAM 16C,15C,14C,13C	–	–	–	–	–	–
1FFF 0000	8K	RAM 12G,13G,14G,15G	–	–	–	–	–	–
Setting inside expansion unit SW2	1	–	OFF	OFF	ON	ON	OFF	OFF
	2	–	OFF	ON	OFF	OFF	OFF	ON
	3	–	ON	ON	ON	OFF	OFF	OFF
	4	–	OFF	OFF	OFF	ON	ON	ON
Jumper	J1		A	A	A	B	B	B
	J2		A	A	A	B	B	B

* The expansion unit is originally set as follows before shipment form the factory.

Jumpers { J1 : B ; J2 : B }

DIP switch (SW2) { 1 : ON ; 2 : OFF ; 3 : OFF ; 4 : ON }

- SWTCH 1 (SW1) turns on and off the Vc voltage line through which Vc voltage is supplied from the HX-20. The Vc voltage line carries a voltage of approximately +5V when power is on, and drives the elements connected to the Vc line.
  The Vc voltage line also outputs a voltage of approximately +3V when power is off so that it may also be used for memory backup. The eight RAMs and IC1A in the expansion unit use this Vc voltage, which protects the data stored in the RAMs, and controls the RAM CE2 signal and reset signal.
  * Be sure to set this switch to the ON position before use.



IC TYPE	USAGE LOCATION
40H000	1A 5A
40H002	3A 6A
40H004	7A
40H010	4A
40H138	2A 8A
40H367	9A 10A 11A
40H245	12A

* CAUTION
IC '1A' MARKED WITH ASTARISK AND DOUBLE LINE IS ALWAYS BATTERY BACKED UP.

HC(X)-20 EXP BOARD
UNIT No. Y202204000